

FIGURE 1

FIG. 2 is a schematic diagram of a memory array structure. The array is organized into rows and columns. Each row is controlled by a Row Control Logic block (110) which provides a row address (102) to the array. Each column is controlled by a Column Control Logic block (112) which provides a column address (103) to the array. The array consists of a grid of memory cells (108) arranged in rows and columns. Each memory cell (108) is connected to a row line (108aa, 108ab, 108da, 108db, 108ad, 108dd) and a column line (108aa, 108ab, 108da, 108db, 108ad, 108dd). The memory cells are connected to the row lines via access transistors (178) and to the column lines via data transistors (178). The data transistors are connected to the column lines via data lines (180, 181, 183). The access transistors are connected to the row lines via word lines (178). The data lines are connected to the column lines via data lines (180, 181, 183). The access transistors are connected to the row lines via word lines (178). The data lines are connected to the column lines via data lines (180, 181, 183). The access transistors are connected to the row lines via word lines (178). The data lines are connected to the column lines via data lines (180, 181, 183).

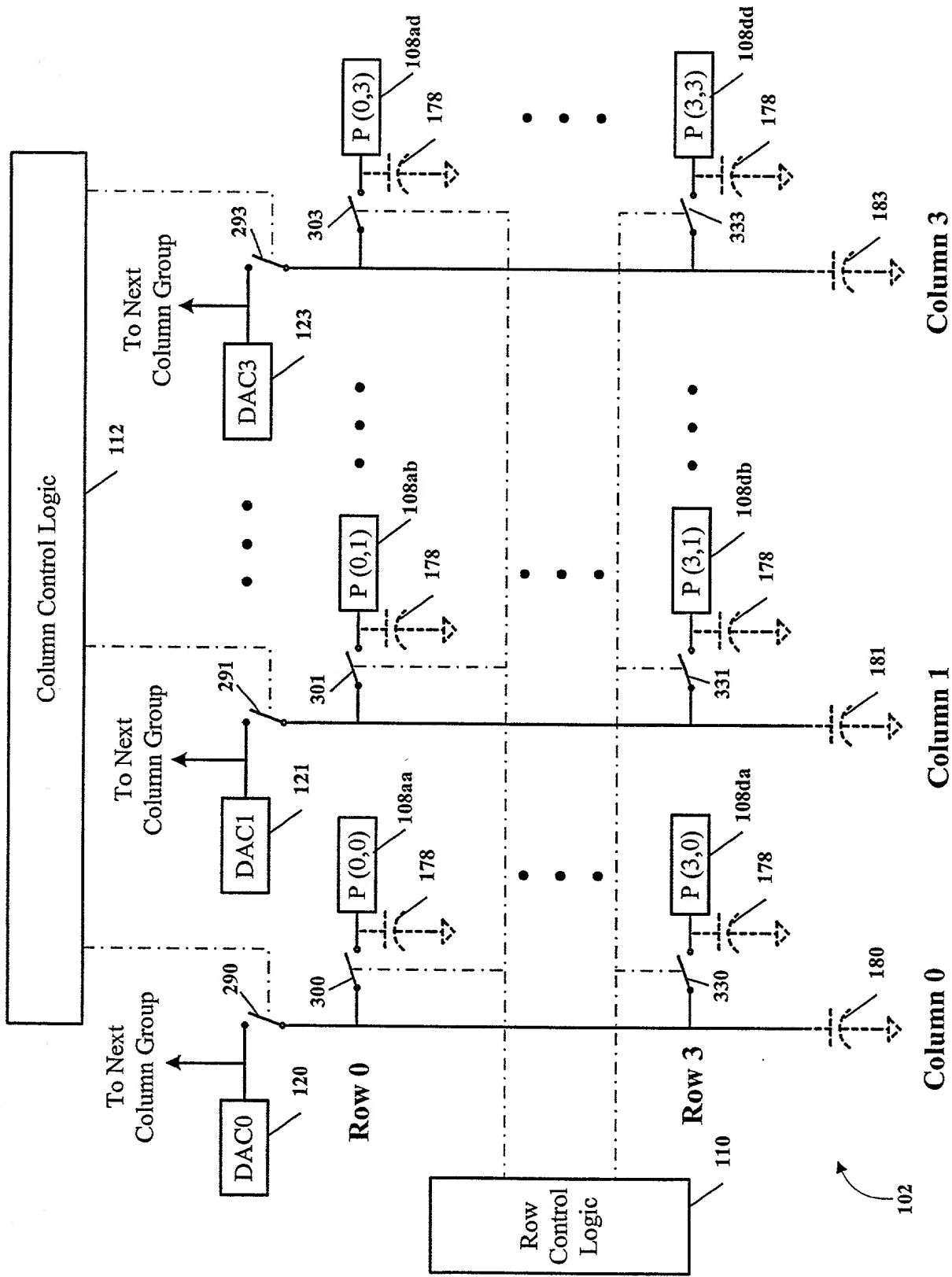


FIGURE 2

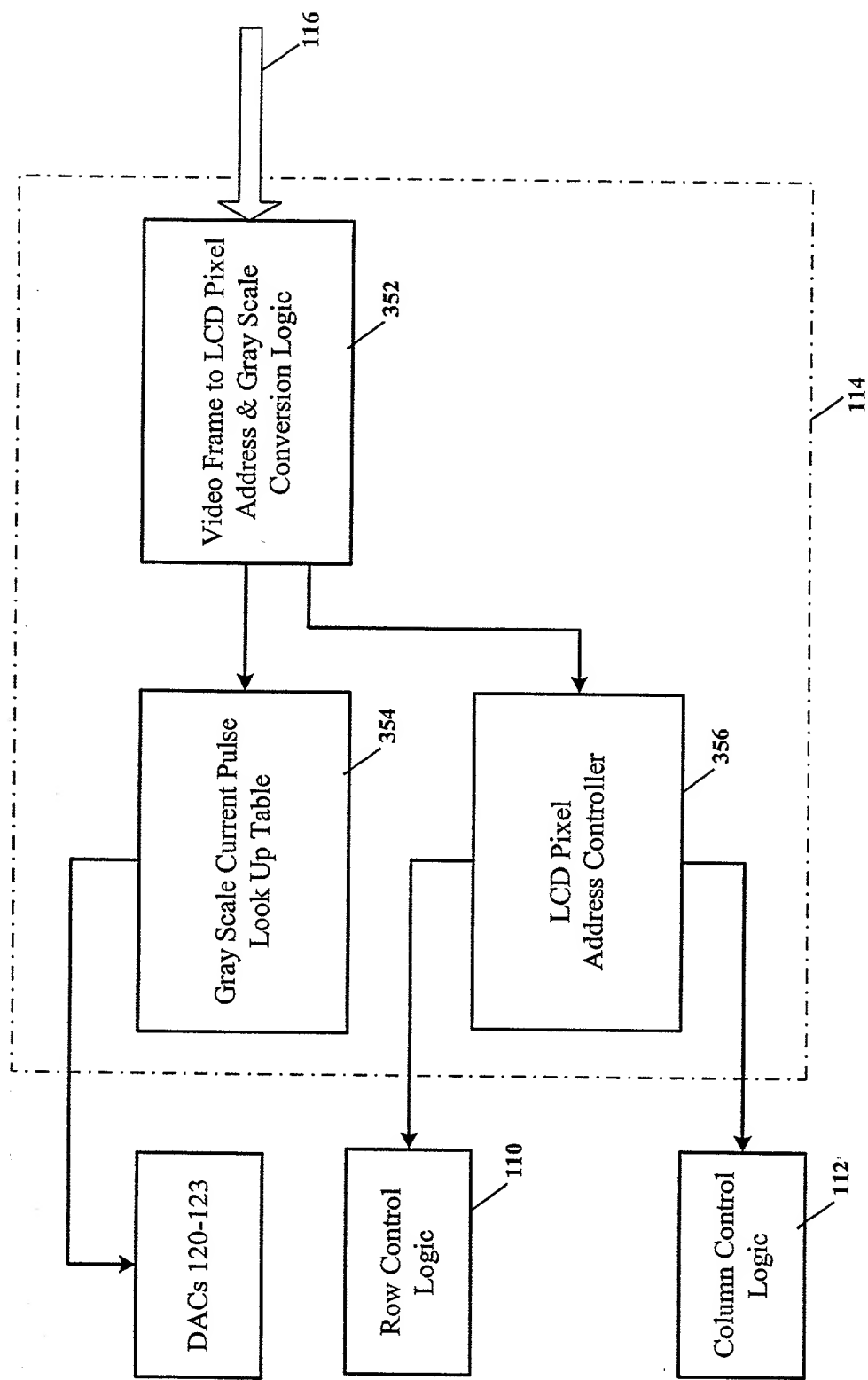


FIGURE 3

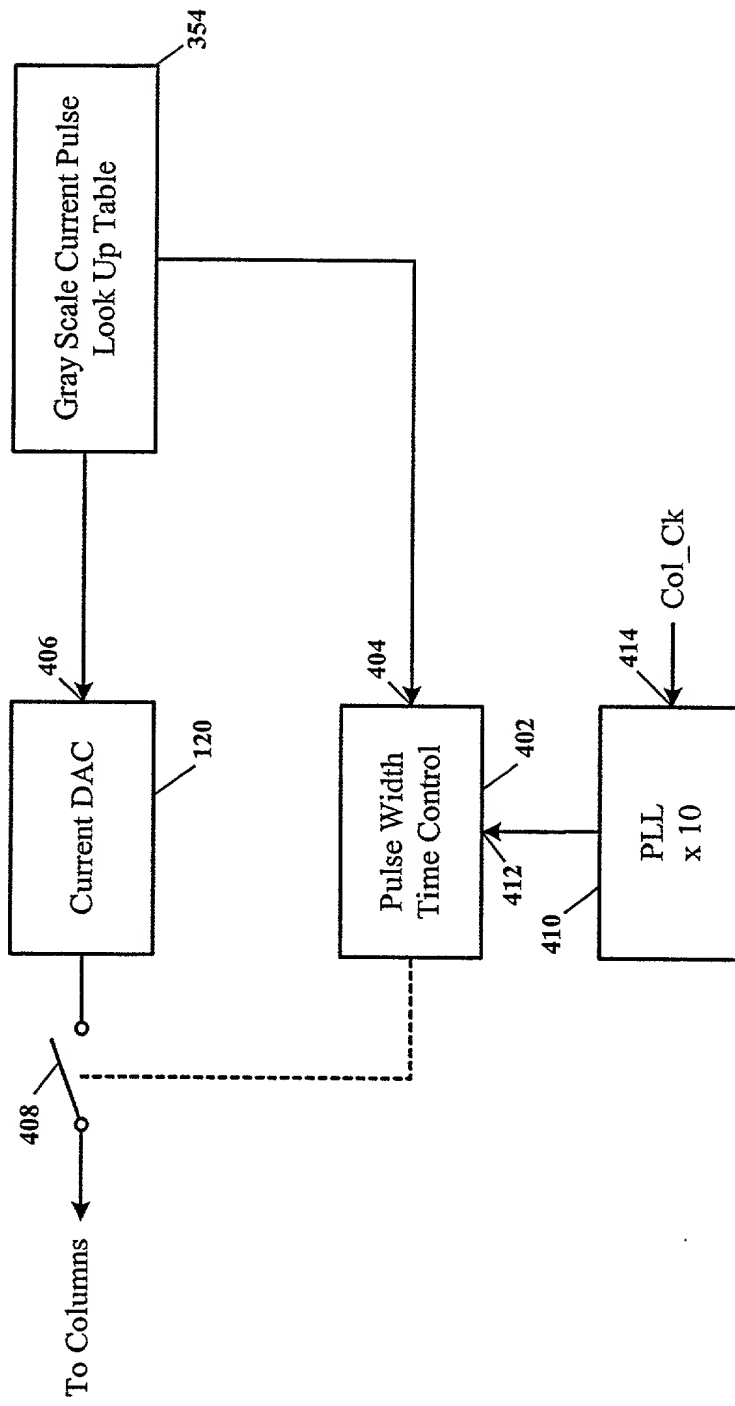


FIGURE 4

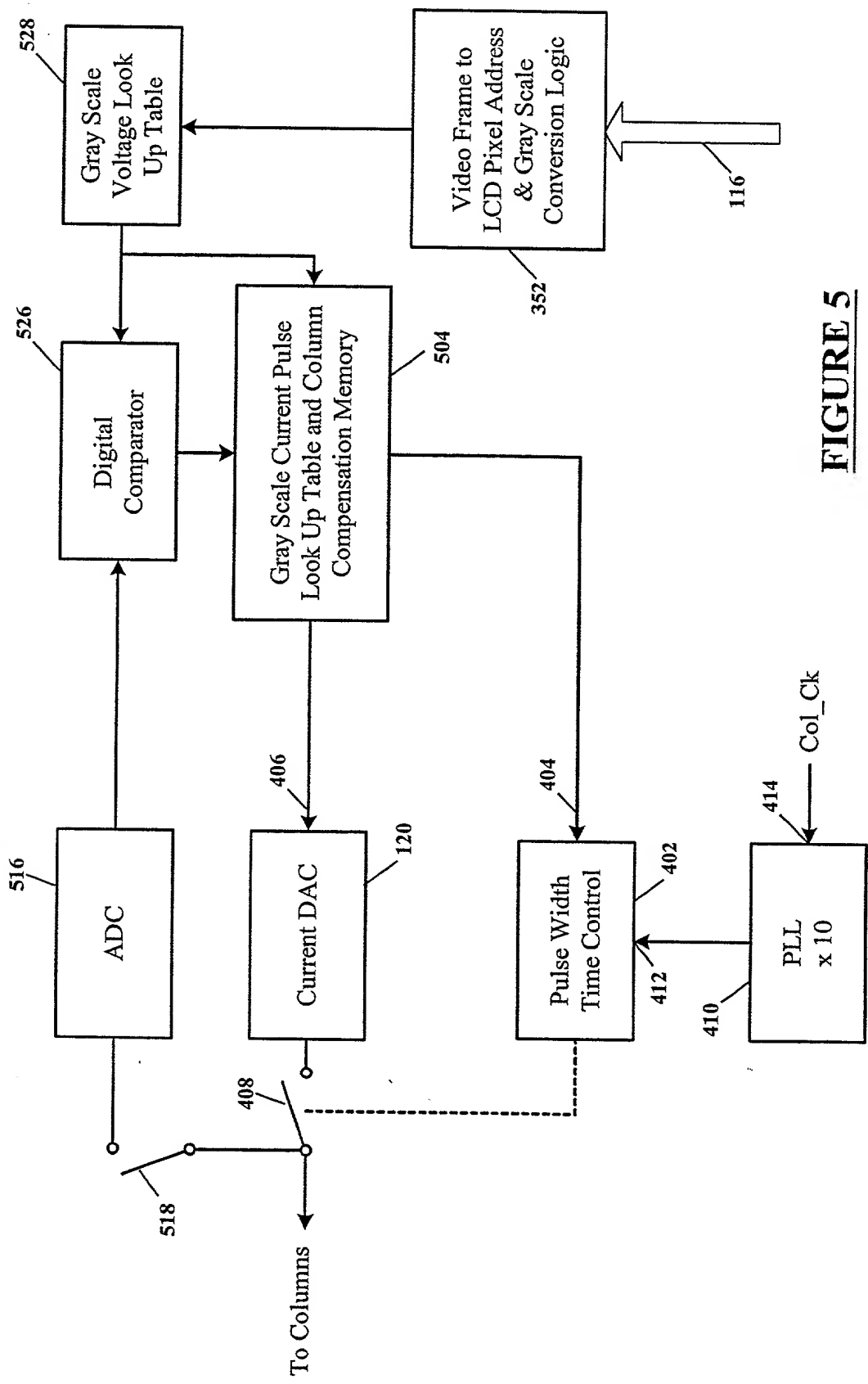


FIGURE 5

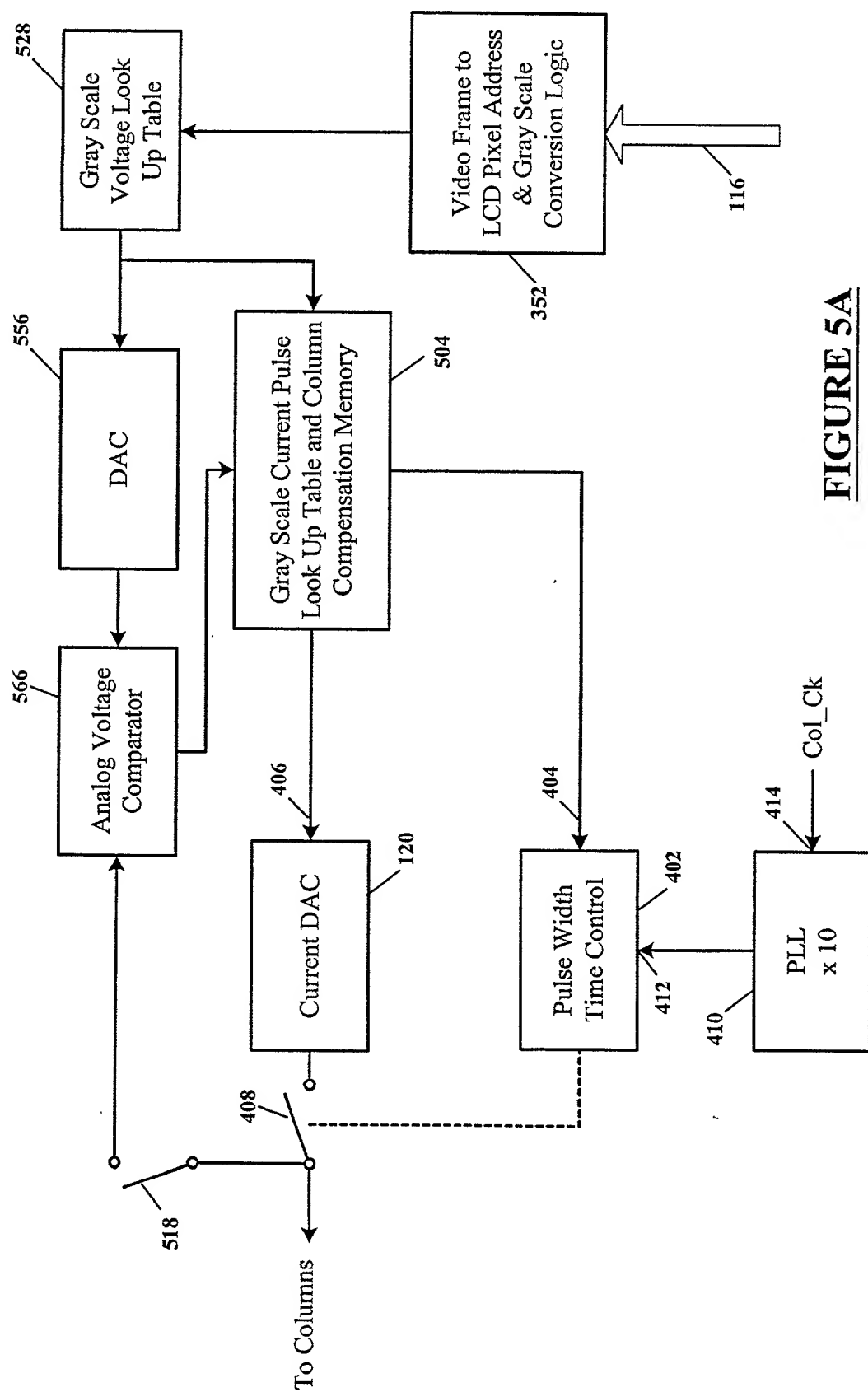


FIGURE 5A

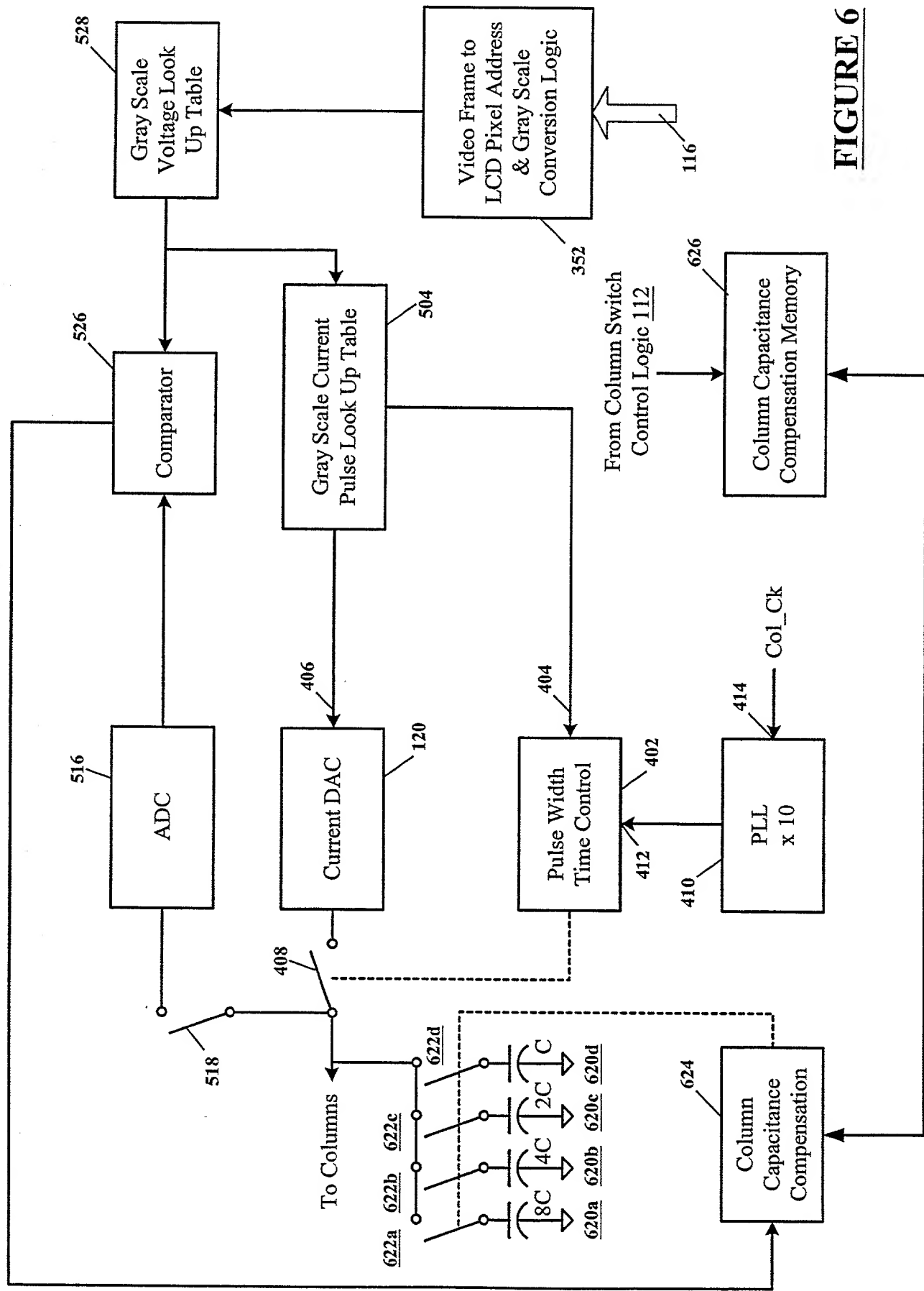


FIGURE 6

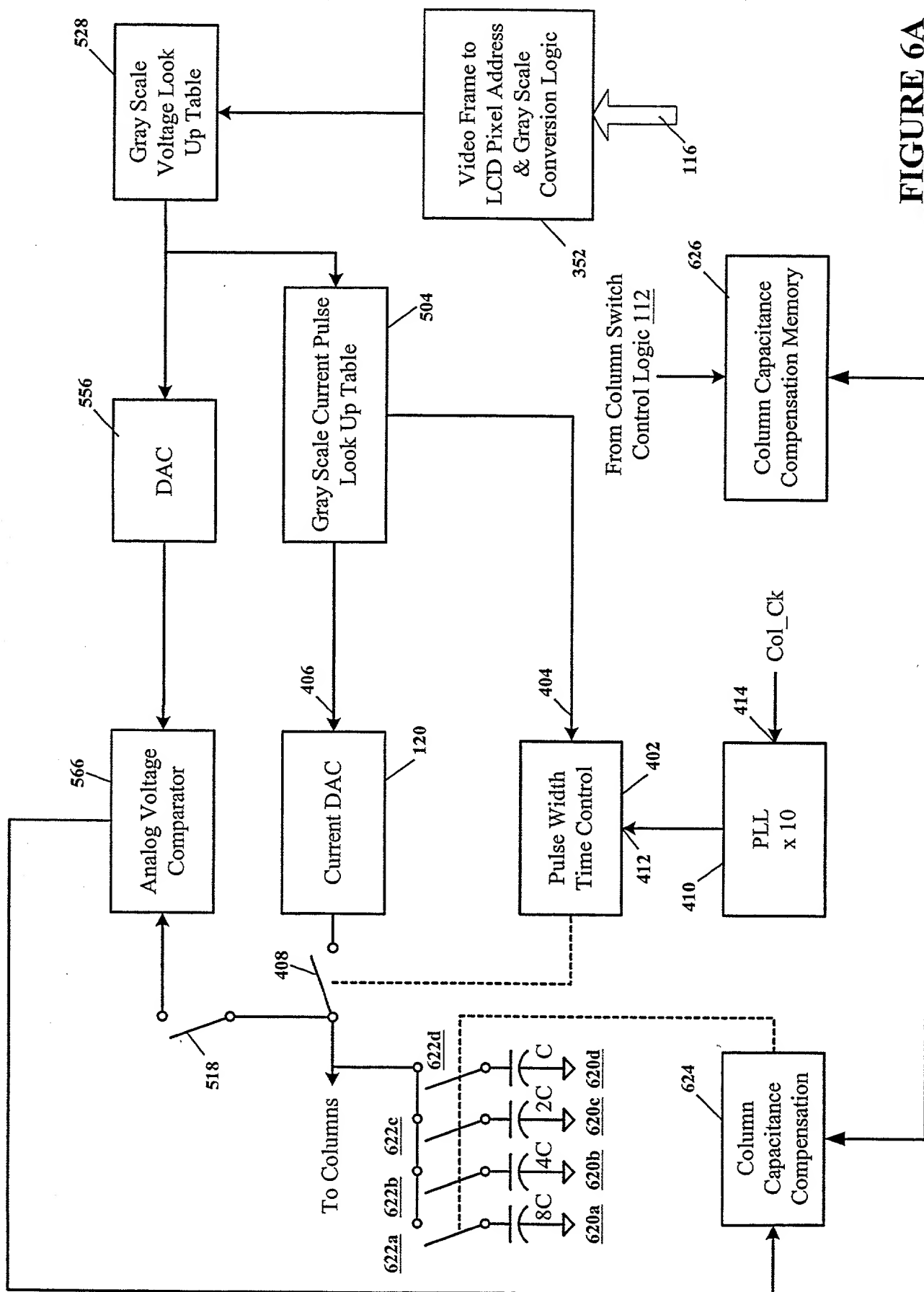


FIGURE 6A

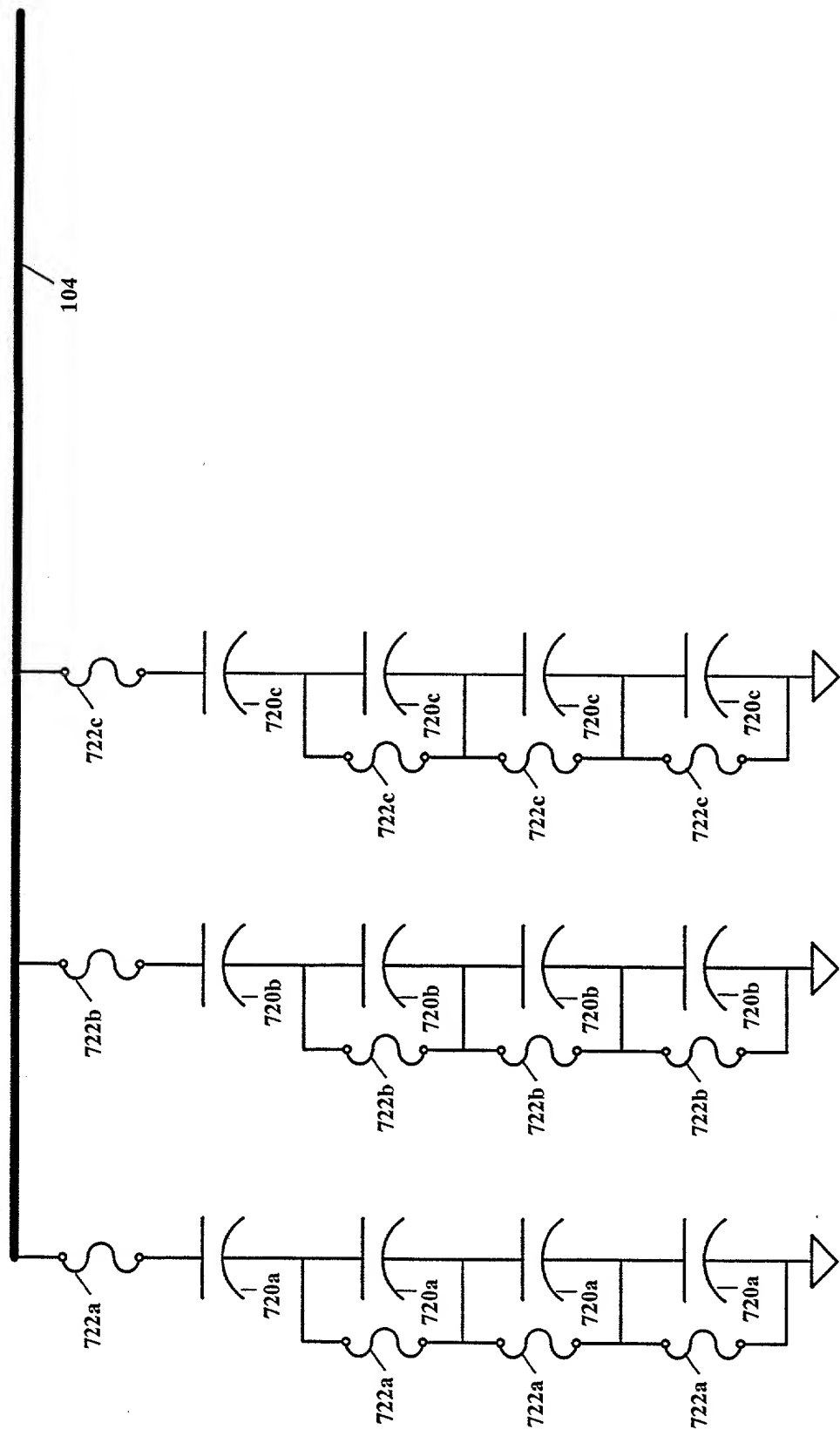


FIGURE 7